Jurnal Sri Wiwoho Mudjanarko 20

by Sri Wiwoho Mudjanarko

Submission date: 01-Jul-2020 05:58PM (UTC+1000)
Submission ID: 1352139993
File name: 20._Jurnal_Sri_Wiwoho.pdf (414.24K)
Word count: 2423
Character count: 13308

International Journal of Engineering & Technology, 7 (2.6) (2018) 327-330

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research Paper

Modeling of A Single Phase 7-Level Cascaded H-Bridge Multilevel Inverter

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Abstract

Recently, almost all industrial devices are mostly built on electronic devices which are precisely sensitive to harmonic. In order to meet the requirement from the industries demand aimed at a free-harmonics and high power rating source is remarkably increased in past few years. An inverter which a device or electric circuit that convert direct current to alternating current is one of the electronic devices that give concern to researchers for improvement of generating a neat power source. The inverter can be categorized into a single level and multilevel inverter. As compared to single level inverter, multilevel inverter offers minimum harmonic distortion and higher power output. This paper presents a model of multilevel inverter using 7-level Cascaded H-Bridge of multilevel DC-AC inverter to reduce total harmonic distortion with different sinusoidal pulse width modulation such as phase disposition and phase opposition disposition. Simulation output of single phase multilevel inverter cascaded H-bridge are analysed and verified in the Matlab/Simulink software. The result show that the 7-level cascaded H-Bridge multilevel inverter with phase disposition technique generate less total harmonic distortion if it is compared to the phase opposition disposition technique.

Keywords: *Cascaded H-Bridge Multilevel Inverter, Total Harmonic Distortion, SPWM- Sinusoidal Pulse Width Modulation, SPWM disposition and SPWM phase opposition disposition technique.*

1. Introduction

Recently, the increasing number of electrical energy loads causes the increasing consumption of fossil fuel. This high consumption will affect the increasing of environment pollution. Besides, due to concern toward pollutions and insufficient of conventional energy resources many countries change over to renewable energy sources. Among these sources, solar energy is on attention because of the unlimited power, pollution free, reliability and low maintenance cost [1][2][3][4][5].

Concerning the DC-AC stage efficiency of energy conversion, the multilevel inverters have attracted attentions over years as a good solution for solar energy system [6][7]. Multilevel Inverter is one of the possible solution which is applicable in many application system. They are capable to use in high voltage application with low harmonic also and easily provide the require power levels needed by the high voltage drives. Hence, they have the capability to ease the waveforms of output voltage with a greater harmonic spectrum.

The term of multilevel inverter start with three levels is introduced [8][9]. As the number of inverter level is increased the output voltage steps, the output is generated with low harmonic distortion. The standard Total Harmonic Distortion (THD) value provided by IEEE Std 519-1992, THD limitations for specific equipment has to be 5% with the filter and 15-25% without a filter can be accomplish by using carrier or space vector based method [10]. However, by increasing number of level lead to complexity of circuit when high number of switches is needed. This paper present a modeling of a seven-level cascaded H-bridge inverter and performance verification of the inverter in different Sinusoidal Pulse Width Modulation (SPWM) control techniques.

2. A seven-level cascaded H-bridge inverter design

Multi Level Inverters (MLI) has developed into wide and great deal of technology. Day by day, there are hundred thousand of inverters available all over the world but multilevel inverters come with great advantages and abilities. One of them is Cascaded H-Bridge inverter (CHB). Comprehensively, the advantages of CHB multilevel inverter are focusing in the improvement of output signal quality and overcome the high risk damage of power device damage for being failed to achieve desired voltage and current rating. Multilevel inverter are developed in way to overcome some limitations of the conventional inverter with some impressive features which is good including capable to generate output voltage and draw current with lowest distortion and can operate at low switching frequency. The proposed a single phase 7-level CHB MLI in this paper is shown in Figure 1.

The single phase 7-level CHB MLI has generated seven step of output as multiplication of it input voltage source (Vdc), such as 3Vdc, 2Vdc, Vdc, 0, -Vdc, -2Vdc and -3Vdc. The resulting AC output voltage swing from +3Vdc to -3Vdc through zero level.

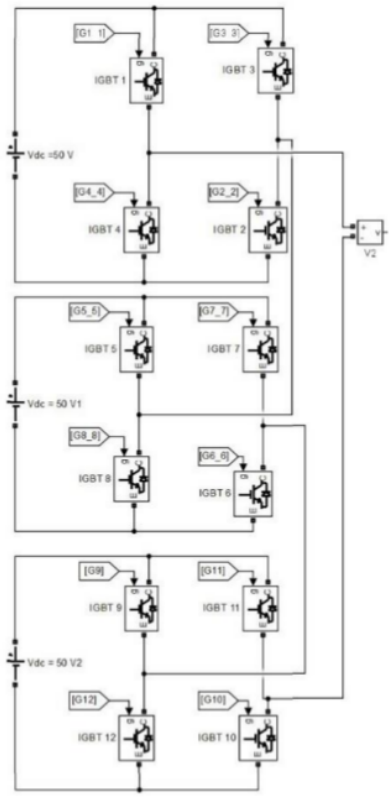

Fig. 1: The proposed a single phase 7-level CHB-MLI configuration

Operation of MLI is determined based on the condition of the switch-closed and switch-open state of each semiconductor devices. Configuration of the switching state will determine output value of the inverter. In the seven -level CHB-MLI there are seven possibilities configuration of the switching state. The output voltage of each configuration can be explained as follow:

State-1:

In this operation the IGBT-1, IGBT-2, IGBT-5, IGBT-6, IGBT-9 and IGBT-10 are closed, hence the output voltage is 3 time of Vdc.

State-2:

In this operation the IGBT-1, IGBT-2, IGBT-5, IGBT-6, IGBT-10 and IGBT-12 are closed, hence the output voltage is 2 time of Vdc.

State-3:

In this operation the IGBT-1, IGBT-2, IGBT-6, IGBT-8, IGBT-10 and IGBT-12 are closed, hence the output voltage is Vdc.

State-4:

In this operation the IGBT-2 IGBT-4, IGBT-6 IGBT-8 IGBT-10 and IGBT-12are closed, hence the output voltage is 0 volt.

State-5:

In this operation when IGBT-2 IGBT-4, IGBT-6 IGBT-8, IGBT-9 and IGBT-10 are closed, hence the output voltage is –Vdc (negative polarity).

State-6:

In this operation when IGBT-2 IGBT-4, IGBT-7 IGBT-8, IGBT-11 and IGBT-12 are closed, hence the output voltage is 2 time of –Vdc (negative polarity).

State-7:

In this operation when IGBT-3 IGBT-4, IGBT-7 IGBT-8, IGBT-11 and IGBT-12 are closed, hence the output voltage is 3 time of –Vdc (negative polarity).

The output voltage of m-level inverter is sum of output of all bridges connected in series. 7-level inverter consists of three bridges that connected in series. The number of level of output in CHB-MLI is given as m=2s+1 where s is separate DC sources and m is the level of inverter. The main function of this inverter is to synthesize desired voltage from separate DC sources.

As the term is known, CHB-MLI is designed with configuration in series with parallel connection of semiconductor switches. A separated number of DC supplies are required by CHB-MLI, each of which feeds an H-bridge power cell. Since the inverter consists of three full H-bridge, then it is required three DC sources for every single H-bridge.

Multicarrier PWM technique is used to control switching pattern of multilevel inverter. In multilevel inverter the techniques are classified as single phase SPWM and multi-carrier SPWM

Meanwhile, Multi-Carrier is classified further as level shifted, phase shifted, hybrid. In Level Shifted, the three technique have been explained [11][12].

2.1. The SPWM – phase disposition scheme

Phase Disposition (PD) technique contains a number of carriers (m-1) where m is the number of level. The PD carriers are in phase accordingly. Regarding simulation of 7-level CHB-MLI, all the six carrier waves are phasing each other and compared to the reference signal.

2.2. The SPWM – phase opposition disposition scheme

Phase Opposition Disposition (POD) introduced the techniques of carriers (m-1) where the top and bottom carriers of the zero reference are in phase. Regarding the simulation 7-level CHB-MLI, the six carrier waves are 180° phase shifted between one of the top and bottom zero reference.

3. Simulation result and discussion

The circuit of single phase 7-level CHB-MLI using Matlab/Simulink is shown in Figure 2. This model consists of two parts, IGBT circuit part and SPWM signal generator module. The simulation of single phase 7-level CHB-MLI is performed at 150V input DC voltage, 5 kHz switching frequency and 50Hz modulating frequency

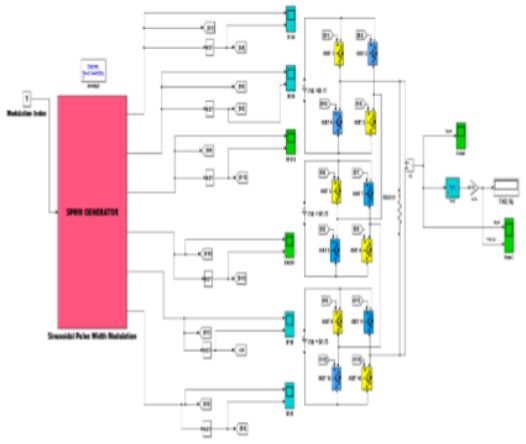

Fig. 2: The single phase 7-level CHB-MLI model

3.1. The RMS output voltage and current

The simulation is performed by using the R load where R= 50Ω for every inverters and the result m-level inverters are obtained at unity modulation index. As 150V DC supply with separated sources where V1=50V, V2= 50V and V3=50V. Comparison of the output voltage and output current of the 7-level, the 5-level, 3-level and 2-level inverter at unity modulation index are shown in Figure 3 and Figure 4 respectively.

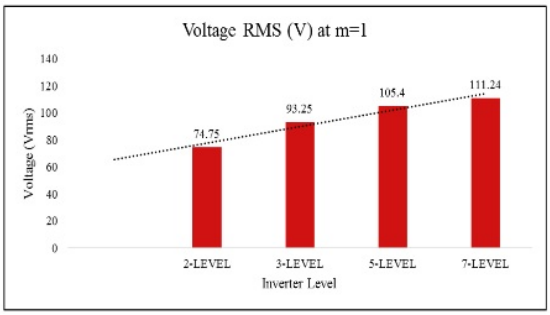

Fig. 3: RMS output voltage at unity modulation of 7-level CHB-MLI

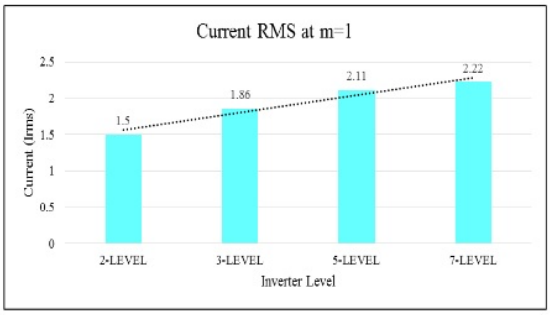

Fig. 4: RMS output current at unity modulation of 7-level CHB-MLI

Referring to the Figure 3 and Figure 4, the RMS output voltage

and current are proportional to number of the level. The maximum RMS output voltage of the 7-level CHB-MLI is 112.4V. The maximum output voltage of the 7-level CHB-MLI is 2.22A

3.2. The output voltage and current waveform

A result of comparison between different carrier signal techniques to generate switching pulse for 7-level inverters using PD and POD modulating signal are verified. The modulating signal of 50Hz and carrier signal frequencies 5 kHz of the SPWM-PD is shown in Figure 5.

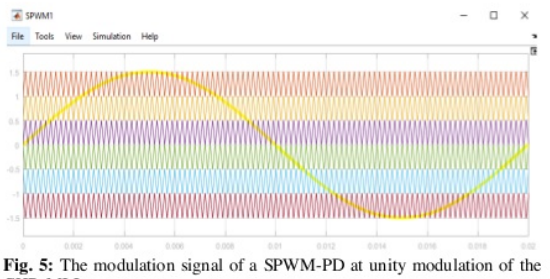

Fig. 5: The modulation signal of a SPWM-PD at unity modulation of the CHB-MLI

The output voltage waveform using SPWM-PD is shown in Figure 6.

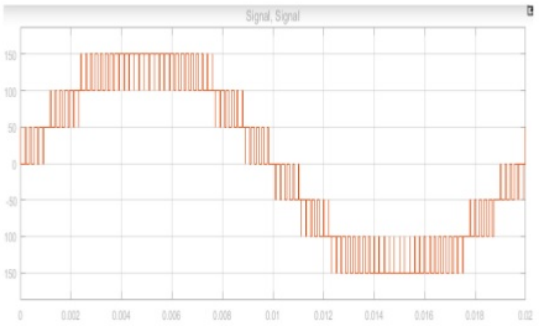

Fig. 6: The output voltage waveform of the CHB-MLI at unity modulation using SPWM-PD technique

The modulating signal of 50Hz and carrier signal frequencies 5 kHz of the SPWM-POD is shown in Figure 7.

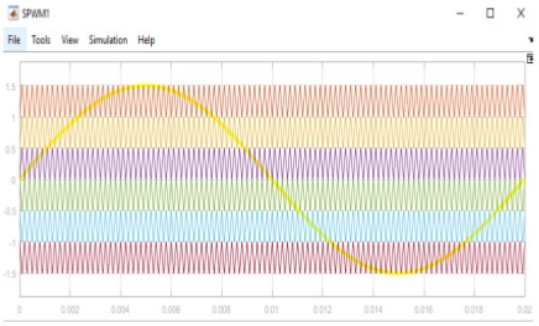

Fig. 7: The modulation signal of a SPWM-POD at unity modulation of the CHB-MLI

The output voltage waveform using SPWM-PD is shown in Figure 8.

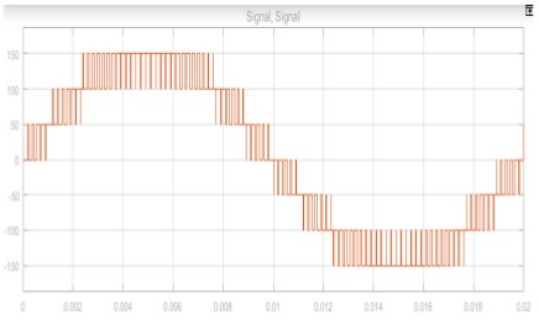

Fig. 8: The output voltage waveform of the CHB-MLI at unity modulation using SPWM-POD technique

3.3. THD performance

In order to verify the THD performance of the CHB-MLI, different values of modulation index are employed. The THD value of the 7-level, 5-level, 3-level and 2-level CHB-MLI in different modulation index from 0.8 up-to unity operations using SPWM-PD technique are shown in the Figure 9. The switching frequency

is kept at 5 kHz to maintain low switching losses [13], meanwhile the frequency of modulating signal is kept at 50Hz.

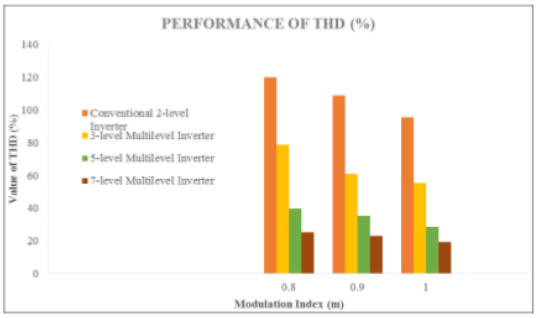

Fig. 9: THD value of the m-level inverters using SPWM-PD signal modulation technique

The THD value for each m-level is proportional to number of the inverter level. On other side, based on the modulation index value the THD of the inverter is decrease when the modulation index is increased. The minimum THD occur at unity modulation index of the 7-level CHB-MLI inverter. Referring to the table 1, the poorer THD occur at low modulation index and low inverter level.

Comparison of the THD value of the seven level CHB-MLI with different switching signal methods by using SPWM-PD technique and SPWM-POD technique is shown in Table 2.

Table 2: THD value of the seven-level inverters using SPWM-PD verses SPWM-POD signal modulation technique

m	THD (%)	
	SPWM PD	SPWM POD
1	19.28	19.33
0.9	23.1	28.89
0.8	25.21	55.41

4. Conclusion

The simulation result for single phase 7-level CHB-MLI with various SPWM control techniques is presented here with help of Matlab/Simulink software. Referring to the result it is shown that the THD value of the multi level inverter is proportional to modulation index and inverse proportional to the number of the inverter level. Based on the switching signal methods, the THD of the SPWM-PD switching signal method less if compare to the SPWM-POD switching signal method.

Acknowledgement

The authors would like express their gratitude to Universiti Tun Hussein Onn Malaysia and Universitas Narotama Surabaya, Indonesia for their support on this project.

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